AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 10, line22 as follows:

--In the packet processing circuit shown in FIG. 3, user blocks 101, 102, and 103 have output routes R1 and R2 of two packets ~~SOP#1~~ SOP#0 and ~~SOP#2~~ SOP#1 and respective associated data DATA#0 and DATA#1.---